Amendments to the Claims:

Please amend claims 42 and 62 as follows. Please cancel claims 68-71 without prejudice. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing:

1. (Previously Presented) A deformable mirror system, comprising:

a deformable mirror being mechanically operated by at least one actuator, said at least one actuator having a signal electrode and a reference electrode, said at least one actuator converting an electrical signal into a mechanical motion, said at least one actuator continuously receiving said electrical signal from an amplifier continuously coupled to the signal electrode of said at least one actuator; and

electronics having at least one switch electrically coupled between said reference electrode and a reference node, said at least one switch defined by at least two selectively controllable solid state switches connected in series and operatively combining to provide a closed state and an open state for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror.

2. (Original) The deformable mirror system according to Claim 1, wherein subsets of actuators are coupled to different amplifiers.

3. (Original) The deformable mirror system according to Claim 1, wherein said reference node is electrically coupled to analog ground.

4. (Original) The deformable mirror system according to Claim 1, wherein the electronics further comprise addressing circuitry electrically coupled to said at least one switch.

5. (Original) The deformable mirror system according to Claim 4, wherein the addressing circuitry comprises circuitry to select zones of switches.

6. (Original) The deformable mirror system according to Claim 1, wherein the electronics further comprise at least one amplifier to provide an electrical signal to the signal electrodes of a subset of actuators.

7. (Original) The deformable mirror system according to Claim 1, wherein the electronics further comprise at least one processor to control the state of said at least one switch.

8. (Original) The deformable mirror system according to Claim 7, wherein said processor receives data from an external system.

9. (Original) The deformable mirror system according to Claim 7, wherein said electronics further comprise at least one amplifier, said at least one processor providing command signals to said at least one amplifier.

10. (Original) The deformable mirror system according to Claim 9, wherein said at least one processor commands said at least one amplifier to apply a desired surface figure to the mirror.

11. (Original) The deformable mirror system according to Claim 9, wherein the electronics comprises at least two processors, at least one processor providing command signals for said at least one amplifier, at least one other processor selecting the states of said at least one switch.

12. (Original) The deformable mirror system according to Claim 7, wherein said at least one processor selects the states of switches configured in zones of switches.

13. (Original) The deformable mirror system according to Claim 7, wherein the electronics comprise a plurality of amplifiers, said at least one processor commanding amplifiers providing electrical signals to actuators configured in respective zones of actuators.

14. (Original) The deformable mirror system according to Claim 7, wherein said at least one processor executes at least one adaptive optics computation.

15. (Original) The deformable mirror system according to Claim 1, wherein the electronics comprise at least one current limiting element.

16. (Canceled)

17. (Previously Presented) The deformable mirror system according to Claim 1, wherein said at least one switch, when in an open state, substantially limits forward and reverse leakage current.

18. (Original) The deformable mirror system according to Claim 17, wherein one of said two solid state switches is an N-Channel MOSFET and the other of the two solid state switches is a P-Channel MOSFET.

19. (Original) The deformable mirror system according to Claim 17, wherein one of the two solid state switches is an N-channel FET having a source (Sn), a drain (Dn), and a gate (Gn), and the other of the two solid state switches is a P-channel FET having a source (Sp), a drain (Dp), and a gate (Gp), wherein:

(i) Dn is electrically coupled to said actuator reference electrode;

(ii) Sn is electrically coupled to Dp;

(iii) Sp is electrically coupled to the reference node; and

(iv) Gn and Gp are electrically coupled to circuitry to apply at least one signal to selectably close and open said at least one switch.

20. (Original) The deformable mirror system according to Claim 17, wherein one of the two solid state switches is an N-channel FET having a source (Sn), a drain (Dn), and a gate (Gn), and the other of the two solid state switches is a P-channel FET having a source (Sp), a drain (Dp), and a gate (Gp), wherein:

(i) Dp is electrically coupled to said actuator reference electrode;

(ii) Sp is electrically coupled to Dn;

(iii) Sn is electrically coupled to the reference node; and

(iv) Gp and Gn are electrically coupled to circuitry to apply at least one signal to selectably close and open said at least one switch.

21. (Previously Presented) A deformable mirror system, comprising:

a deformable mirror being mechanically operated by at least one actuator, said at least one actuator having a signal electrode and a reference electrode, said at least one actuator converting an electrical signal into a mechanical motion, said at least one actuator continuously receiving said electrical signal from a signal means continuously coupled to said signal electrode of said at least one actuator; and

means for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror, said means defined by at least two selectively controllable means connected in series and operatively combining to perform the enabling and disabling of said at least one actuator.

22. (Previously Presented) An apparatus for controlling a deformable mirror mechanically operated by at least one actuator, said at least one actuator having a signal electrode and a reference electrode, the apparatus comprising:

electronics coupled to said reference electrode of said at least one actuator, said electronics having at least one switch electrically coupled between said reference electrode of said at least one actuator and a reference node, said signal electrode of said at least one actuator continuously receiving an electrical signal, said at least one switch defined by at least two selectively controllable solid state switches connected in series and operatively combining to provide a closed state and an open state for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror.

23. (Original) The apparatus according to Claim 22, wherein subsets of actuators are coupled to different amplifiers.

24. (Original) The apparatus according to Claim 22, wherein said reference node is electrically coupled to analog ground.

25. (Original) The apparatus according to Claim 22, further comprising addressing circuitry to select said at least one switch.

26. (Original) The apparatus according to Claim 25, wherein the addressing circuitry comprises circuitry to select zones of switches.

27. (Original) The apparatus according to Claim 22, wherein the electronics further comprise at least one amplifier to provide electrical signals to the signal electrodes of a subset of actuators.

28. (Original) The apparatus according to Claim 22, wherein the electronics further comprise at least one processor to control the state of said at least one switch.

29. (Original) The apparatus according to Claim 28, wherein the processor receives data from an external system.

30. (Original) The apparatus according to Claim 28, wherein the electronics further comprise at least one amplifier, said at least one processor providing command signals to said at least one amplifier.

31. (Original) The apparatus according to Claim 30, wherein said at least one processor commands said at least one amplifier to apply a desired surface figure to the mirror.

32. (Original) The apparatus according to Claim 30, wherein the electronics comprise at least two processors, at least one processor providing command signals for said at least one amplifier, at least one other processor selecting the states of said at least one switch.

33. (Original) The apparatus according to Claim 28, wherein said at least one processor selects the states of switches configured in zones of switches.

34. (Original) The apparatus according to Claim 28, wherein the electronics comprise a plurality of amplifiers, said at least one processor commanding said amplifiers providing electrical signals to said actuators configured in zones of actuators.

35. (Original) The apparatus according to Claim 28, wherein said at least one processor executes at least one adaptive optics computation.

36. (Original) The apparatus according to Claim 22, wherein the electronics comprises at least one current limiting element.

37. (Original) The apparatus according to Claim 22, wherein said at least one switch is composed of at least one solid state switch.

38. (Original) The apparatus according to Claim 22, wherein said at least one switch is composed of two solid state switches providing (i) a closed state having a low impedance and (ii) an open state limiting forward and reverse leakage current.

39. (Original) The apparatus according to Claim 38, wherein one of the two solid state switches is an N-Channel MOSFET and the other of the two solid state switches is a P-Channel MOSFET.

40. (Original) The apparatus according to Claim 38, wherein one of the two solid state switches is an N-channel FET having a source (Sn), a drain (Dn), and a gate (Gn), and the other of the two solid state switches is a P-channel FET having a source (Sp), a drain (Dp), and a gate (Gp), wherein:

(i) Dn is electrically coupled to the actuator reference electrode;

(ii) Sn is electrically coupled to Dp;

(iii) Sp is electrically coupled to the reference node; and

(iv) Gn and Gp are electrically coupled to circuitry to apply at least one signal to selectably close and open said at least one switch.

41. (Original) The apparatus according to Claim 38, wherein one of the two solid state switches is an N-channel FET having a source (Sn), a drain (Dn), and a gate (Gn), and

the other of the two solid state switches is a P-channel FET having a source (Sp), a drain (Dp), and a gate (Gp), wherein:

(i) Dp is electrically coupled to the actuator reference electrode;

(ii) Sp is electrically coupled to Dn;

(iii) Sn is electrically coupled to the reference node; and

(iv) Gp and Gn are electrically coupled to circuitry to apply at least one signal to selectably close and open said at least one switch.

42. (Currently Amended) An apparatus for controlling a deformable mirror mechanically operated by at least one actuator, said at least one actuator comprising a signal electrode and a reference electrode, said at least one actuator receiving an electrical signal at the signal electrode, the apparatus comprising:

means for continuously receiving the electrical signal at the signal electrode; and

means for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror, said means defined by at least two means connected in series for combining to perform the enabling and disabling.

43. (Previously Presented) An apparatus for controlling a deformable mirror mechanically operated by at least one actuator, said at least one actuator comprising a signal electrode and a reference electrode, said at least one actuator receiving an electrical signal at the signal electrode, the apparatus comprising:

electronics coupled to said at least one actuator, the electronics comprising (i) an amplifier having an output continuously coupled to the signal electrodes of said at least one actuator, and (ii) at least one switch electrically coupled between the reference electrode of said at least one actuator and a reference node providing a signal reference, said at least one switch defined by at least two selectively controllable solid state switches connected in series and operatively combining to provide a closed state and an open state for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror;

addressing circuitry to enable at least one switch coupled to the addressing circuitry, the addressing circuitry converting an address signal to a switch selection; and

at least one processor executing processor instructions, the processor instructions comprising instructions to:

issue address signals to the addressing circuitry; and

in coordination with issuing the address signals, direct corresponding actuator commands to the amplifier to supply the electrical signal continuously to the signal electrode of said at least one actuator to mechanically operate the deformable mirror.

44. (Original) The apparatus according to Claim 43, wherein, to coordinate issuing address signals and directing actuator commands, the processor instructions further comprise instructions to:

for a given actuator, direct the amplifier to output a first signal, the first signal corresponding to a signal most recently applied to the given actuator;

issue a first address signal to close a switch corresponding to the given actuator;

direct the amplifier to output a second signal corresponding to the signal determined by the processor to be directed to the given actuator; and

issue a second address signal to open the switch corresponding to the given actuator.

45. (Original) The apparatus according to Claim 43, wherein the instructions further comprise instructions to parse a command frame, the command frame including actuator commands.

46. (Original) The apparatus according to Claim 45, wherein the command frame is received from an external system.

47. (Original) The apparatus according to Claim 45, wherein the instructions further comprise instructions to process the actuator commands in the command frame to limit inter-actuator stroke applied to the mirror.

48. (Original) The apparatus according to Claim 43, wherein the instructions to direct actuator commands to the amplifier comprise instructions to limit current flow through the switches.

49. (Original) The apparatus according to Claim 43, wherein the instructions to issue address signals to the addressing circuitry comprise instructions to issue address signals to the addressing circuitry for zones of actuators.

50. (Original) The apparatus according to Claim 43, wherein the instructions further comprise instructions to conserve power consumed by the apparatus.

51. (Original) The apparatus according to Claim 50, wherein the instructions to conserve power consumed by the apparatus further comprise instructions to retain a figure on the mirror while conserving power consumed by the apparatus.

52. (Original) The apparatus according to Claim 43, wherein the processor includes a plurality of processors.

53. (Previously Presented) A method for controlling a deformable mirror mechanically operated by actuators in an actuator array, the method comprising:

applying a first control signal to a first selectively controllable solid state switch and a second control signal to a second selectively controllable solid state switch connected in series with the first selectively controllable solid state switch, the first and second selectively controllable solid state switches operatively combining to selectably enable or disable at least one actuator by applying a reference signal to a first electrode of said at least one actuator; and

providing a command signal continuously to a second electrode of said at least one actuator to operate the mirror.

54. (Original) The method according to Claim 53, further comprising driving an initial command signal to the second electrode of said at least one actuator prior to applying the reference signal to the first electrode.

55. (Original) The method according to Claim 53, further comprising parsing a command frame, the command frame including actuator commands.

56. (Original) The method according to Claim 55, wherein the command frames are received from an external system.

57. (Original) The method according to Claim 55, further comprising processing the actuator commands in the command frame to limit inter-actuator stroke applied to the mirror.

58. (Original) The method according to Claim 53, wherein driving a command signal to said at least one actuator comprises limiting current flow through the switches.

59. (Original) The method according to Claim 53, further comprising applying a reference signal to first electrodes of actuators configured in a zone of actuators.

60. (Original) The method according to Claim 53, further comprising conserving power consumed.

61. (Original) The method according to Claim 60, wherein conserving power consumed by the apparatus comprises retaining a figure on the mirror while conserving power.

62. (Currently Amended) An apparatus for controlling an assemblage of actuators, the actuators having respective first and second electrodes, the apparatus comprising:

means for continuously driving a command signal to the first electrodes of said actuators; and

means for selectably applying a reference signal to the second electrode of at least one actuator to control said at least one actuator in said assemblage of actuators, said means defined by at least two means connected in series for combining to apply the reference signal.

63. (Previously Presented) An apparatus for controlling a deformable mirror mechanically operated by at least one actuator, said at least one actuator comprising a signal electrode and a reference electrode, said at least one actuator receiving an electrical signal at the signal electrode, the apparatus comprising:

electronics coupled to said at least one actuator, the electronics comprising (i) an amplifier having an output coupled to the signal electrodes of said at least one actuator, and (ii) at least one switch electrically coupled between the reference electrode of said at least one actuator and a reference node providing a signal reference, said at least one switch having a closed state and an open state for selectably enabling and disabling said at least one actuator to control the mechanical operation of the mirror;

addressing circuitry to enable at least one switch coupled to the addressing circuitry, the addressing circuitry converting an address signal to a switch selection; and

at least one processor executing processor instructions, the processor instructions comprising instructions to:

issue address signals to the addressing circuitry; and

in coordination with issuing the address signals, direct corresponding actuator commands to the amplifier to supply the electrical signal to the signal electrode of said at least one actuator to mechanically operate the deformable mirror;

for a given actuator, direct the amplifier to output a first signal, the first signal corresponding to a signal most recently applied to the given actuator;

issue a first address signal to close a switch corresponding to the given actuator;

direct the amplifier to output a second signal corresponding to the signal determined by the processor to be directed to the given actuator; and

issue a second address signal to open the switch corresponding to the given actuator.

64. (Previously Presented) The apparatus according to Claim 63, wherein the instructions further comprise instructions to parse a command frame, the command frame including actuator commands.

65. (Previously Presented) The apparatus according to Claim 63, wherein the instructions further comprise instructions to process the actuator commands in a command frame to limit inter-actuator stroke applied to the mirror.

66. (Previously Presented) The apparatus according to Claim 63, wherein the instructions to direct actuator commands to the amplifier comprise instructions to limit current flow through the switches.

67. (Previously Presented) The apparatus according to Claim 63, wherein the instructions to issue address signals to the addressing circuitry comprise instructions to issue address signals to the addressing circuitry for zones of actuators.

68-71. (Canceled)